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THESIS

EXTENDING OPEN ARCHITECTURE (OA) TO THE PHYSICAL LAYER

by

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March 2008

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EXTENDING OPEN ARCHITECTURE (OA) TO THE PHYSICAL LAYER

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Requirements for the degree of

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from the

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ABSTRACT

The purpose of this thesis is to identify the key parameters and metrics associated with field programmable gate array (FPGA) devices, which can be utilized in future integrated weapon systems (IWS) designs that will offset the costs of time-consuming maintenance and upkeep of the current IWS. The FPGA is a reconfigurable and programmable device, design from commercial off the shelf (COTS) materials, through the Navy's open architecture (OA) procurement process that provides the IWS the necessary capabilities to continue to perform at the highest possible level.

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I. INTRODUCTION

A. PURPOSE

The need for an Open Architecture (OA) approach to guide the replacement of the aging AEGIS Weapons System should not be underestimated. Since 2000, the Navy began utilizing the OA concept in all its acquisition processes, and eventually it became the standard approach for the acquisition of the AEGIS weapon system upgrade. The first step to achieving the new strategy was instituted with the creation of the office of Program Executive Office Integrated Weapon Systems (PEO-IWS). The first head of PEO-IWS Rear Adm. C. Bush stated, “We need to stop building proprietary architectures”.¹ With that change in fundamental approach, the Navy shifted its resources to full utilization of commercial off the shelf (COTS) software.

B. BACKGROUND

The AEGIS weapon system has been deployed onboard naval vessels for nearly three decades. The system’s capabilities are unmatched by any existing maritime forces. As years have passed, the system has been the focus of research to determine a viable solution to its upgrade for future operations. As the effects of budget cuts have targeted other programs, AEGIS is under scrutiny as a solution to its upkeep is sought. The shift from a closed system approach to an open system approach is seen as one possible solution in terms of costs, which include maintenance and upkeep.

Previous thesis research has looked at the OA approach to the AEGIS upgrades. ENS J. Adler’s and ENS J. Ahart’s thesis, June 2007, looked at the potential advantages of software upgrades and the knowledge value added (KVA) it achieved. A comparative analysis of the benefits of their research in using OA to upgrade AEGIS will be used in

¹ Sandra I. Erwin, Navy to Upgrade Aegis Ships With Open Software Standards.

the development of this thesis. Their findings, of a positive ROI in sustaining engineering could be useful in understanding how the use of a newer technology can generate similar results.

In September 2007, LT. Seaman's thesis research examined the potential ROI benefits that could be achieved in the littoral combat ship LCS program. His research emphasized the importance of how any ROI achieved in naval ships construction simply by shifting from closed architecture could not be understated.

The overall approach utilized here will be to look at what can be achieved with OA as the approach to the AEGIS upgrade and the use of the FPGA as the hardware to replace aging computers, which will result in lower costs and more capable combat systems.

C. RESEARCH OBJECTIVES

The objectives of this research will support the hypothesis that open architecture at the hardware level, with FPGA technology, will bring to Naval AEGIS weapon system significant long term cost savings and provide a positive (ROI) that will guide the future approach to AEGIS procurement for generations to come.

D. RESEARCH QUESTIONS

The guiding research question this thesis will answer is:

- How can the existing OA approach be modified to include reconfigurable hardware components at the chip level?
- What are the potential cost savings in the acquisition life cycle by including reconfigurable computing capabilities within the OA framework?

E. METHODS

This thesis will look at the potential benefits FPGA devices can add to the AEGIS systems as the Navy pursues large-scale upgrades. AEGIS systems are being upgraded to

insure the military retains a competitive edge against future enemies. By utilizing FPGAs, the weapon system can continue to provide service with greater technological advances.

F. THESIS ORGANIZATION

This thesis is organized by chapters. Chapter I will study the OA acquisition strategy currently used by the Navy for all its weapon systems upgrades and also contains a detail of FPGA technology. Chapter II will detail the current state of upgrading AEGIS and the potential advantages the use of FPGAs will provide. Chapter III will define ROI and look at a comparative analysis of the use of open architecture for AEGIS software upgrades. Chapter IV details the life cycle costs that are associated with the AEGIS upgrade to the Navy's inventory. Chapter V will provide recommendations and conclude with a summarization of the thesis research. Chapter VI will discuss the limitations.

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II. OPEN ARCHITECTURE

A. OPEN ARCHITECTURE APPROACH FOR NAVAL ACQUISITION

Open Architecture OA is a general term that describes, “plug and play” computing.² The Navy looked to this acquisition approach in an effort to greatly reduce the cost of upgrades for its aging AEGIS weapon system. OA has many benefits such as interchanging of computerized systems, which is very important to the service that is trying to reduce costs of maintaining aging systems and continue with procurement of future weapon systems.

The approach to OA is the use of several vendors for the upgrades to a computer system. The Navy has transitioned from single source proprietary systems, commonly referred to as closed systems, to the open system approach. Closed systems prevent the use of several vendors to contribute to upgrades to a computer system. A closed system is synonymous with increased costs and reduced or little innovation.

To begin the move from closed to open architecture the Navy instituted a new organization with the intent of moving forward with costs reductions and improved computer systems. The new organization had a huge task to remove computer systems that lacked interoperability, computer systems that only had proprietary components, which prevented ease of technical upgrades and produced huge costs, as well as computer operators with few resources to update and upgrade their systems. The PEO-IWS organization initiated open architecture in the Navy. By working with varying civilian companies, the organization became the lead analytical and performance monitor for all standard upgrades to the fleet computing systems.

² Vaughn Betz. and Jonathan Rose. "FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density," 21 (accessed 9/22/2007).

1. Navy Transition to OA

Initial research performed by the Navy into transitioning its assets towards COTS provided valuable insight into the driving factors of transforming the acquisition cycle. The cost to continue upgrades for the aging proprietary computer hardware was a driving factor in replacing the systems with COTS systems. In a response to growing criticism concerning these costs then director of PEO-IWS, Rear Adm. C. Tom Bush stated, “OA is the right way to go, we need to stop building proprietary architectures.”³

For non-revenue generating organization such as the Navy, the idea of driving costs down as new computer system components are procured is important. The need to reduce the budget is key, but at the same time so is the ability of the service to keep pace with civilian technology. “With OA, the system operators could swap hardware components, irrespective of proprietary vendors, and achieve increased levels of interoperability, scalability, reliability, and maintenance of critical systems.”⁴

AEGIS was developed by Lockheed Martin, the lead civilian company contracted with all aspects of research, design, integration, and sustainment of AEGIS. The company outsources to smaller vendors for the development of the newest technology. Lockheed Martin is pushing the OA approach to upgrading AEGIS to include not only software but also hardware. The design of the hardware components will readily allow for upgrades and maintenance, as well as mission flexibility and insulation from other subsystems.

2. Advantages of OA

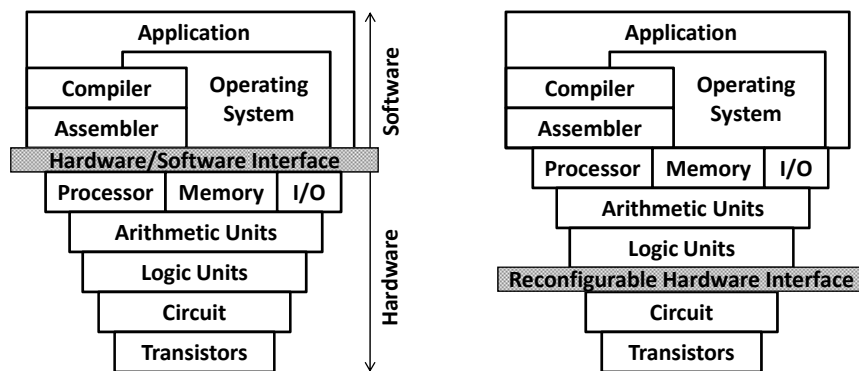
Currently the OA approach to AEGIS upgrades focuses on the software of the computer systems. As with advancing technology in the civilian sector, the trend towards upgrading AEGIS hardware components could similarly provide many of the same

³ Sandra I. Erwin, Navy to Upgrade Aegis Ships with Open Software Standards.

⁴ Arrow Incorporated, White papers for Open Architecture computing.

advantages. As we begin to shift the discussion of the potential benefits achievable with OA hardware keep in mind the benefits currently provided through OA software upgrades.

As it shows in Figure 1, contributed by Dr. Ryan Kastner, Professor of Electrical Engineering at the University of California at San Diego, the desired result of figure 1 is to “increase the flexibility and performance while reducing costs simply by allowing for reconfigurable hardware.”⁵



The left diagram depicts traditional design flow using a microprocessor solution. The solution on the right increases the flexibility and performance as well as reduces the cost of the deployed system by allowing hardware reconfiguration.

Figure 1. Design flow of reconfigurable hardware⁶(From Kastner)

For any Navy units operating at sea, OA at the hardware level could provide the capability of interoperability. Legacy components, which are not compatible with other systems, prevent interoperability and may put the service at risk. OA benefits the Navy by providing for easier and faster upgrades and maintenance of its computing systems.

⁵ Ryan Kastner, on the topic of Extending Open Architecture to the Physical Layer: Implications for Acquisition, personal communication 2007.

⁶ Ryan Kastner, on the topic of Extending Open Architecture to the Physical Layer: Implications for Acquisition, personal communication 2007.

“The potential cost savings of such an approach would save the Navy nearly \$1 billion a year (about 50 percent of its annual upgrade expenditures).”⁷

OA promises yet another advantage to AEGIS hardware upgrades. By making the hardware, independent of the software OA allows for quick maintenance. John Rappisi of Lockheed Martin stated, “The promise of OA is that it makes the hardware independent of the software”.⁸ Because with OA all the hardware that is used is commercial off the shelf (COTS) and has an upgrade path, which is not the case with the original Navy computing systems.⁹

3. Disadvantages of OA

OA is not without its share of possible disadvantages. As stated by retired Rear Adm. G. Meinig, AEGIS technical director in the mid-1980s, “The benefits of OA are desirable, but there is no assurance that unaltered COTS products can meet the performance requirements of the combat system, without careful testing”.¹⁰ The risks of compromising the entire AEGIS suite from one noncompliant design are tremendous.

The use of COTS continues to prove beneficial. For any private sector company the promise of achieving a large government contract for upgrades to the AEGIS system are enormous. The Navy is a large organization with a complex set of rules for proposed budgetary items acquisition. With OA, however, the budget has not fully incorporated the new standards of COTS software. The Navy has to rely heavily on civilian standards of operating and compliance. The key point is in the process of replacing the closed system; the potential for growth is enormous.

⁷ Vaughn Betz and Jonathan, Rose., *FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density*

⁸ Vaughn Betz and Jonathan, Rose., *FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density*

⁹ Ibid.

¹⁰ Sandra I Erwin, [Navy to Upgrade Aegis Ships with Open Software Standards](#), May 2003.

4. Risks

There are potential risks with implementing OA at the hardware level, as there are with many new technological approaches. The Navy has instituted varied programs to mitigate these risks. The programs center on the potential security risks that may arise and are being closely monitored at the highest levels in the acquisition process. As stated, civilian companies must achieve compliance with numerous Navy and department of defense standards before they are awarded contracts to become part of the AEGIS team. The risks of OA are never going to be eliminated but a service wide effort will reduce them to a manageable level.

The focus of the OA approach to upgrading AEGIS is on hardware, so the discussion shifts towards the newest technological innovation, the FPGA. This device, with capabilities that are far superior to current AEGIS components could provide the Navy with many mission critical advantages. The advantages will be discussed and identify the FPGA as the next step in the evolution of computing and how it will benefit the future Navy combat systems.

B. FPGA REVIEW

1. History

Now that we have a general understanding of one potential benefit, interoperability, the Navy could achieve by extending OA to the hardware level in the form of reconfigurable FPGAs, let us review to see how programmers and designers developed the technology.

The history of FPGA technology can be traced back decades, when the first attempts at reconfigurable hardware began. We begin at the basic components of the architecture of computers. It starts with the nonprogrammable application specific integrated circuit (ASIC), followed by the programmable logic device (PLD), the programmable gate array (PGA) and finally the emergence of the FPGA.

The development of reconfigurable hardware begins with the most basic building block of a computing system. Early units consisted of simple circuitry and had little memory. Figure 2 below shows the three levels of computational architecture hierarchy. The basic level is shown as the gate level where the initial computer systems operated with bits. As we move along in technology, the advances moved to larger and more complex operations and the byte. Finally, the instruction sets (up to 128 bits) could be reconfigurable through the bus and memory.

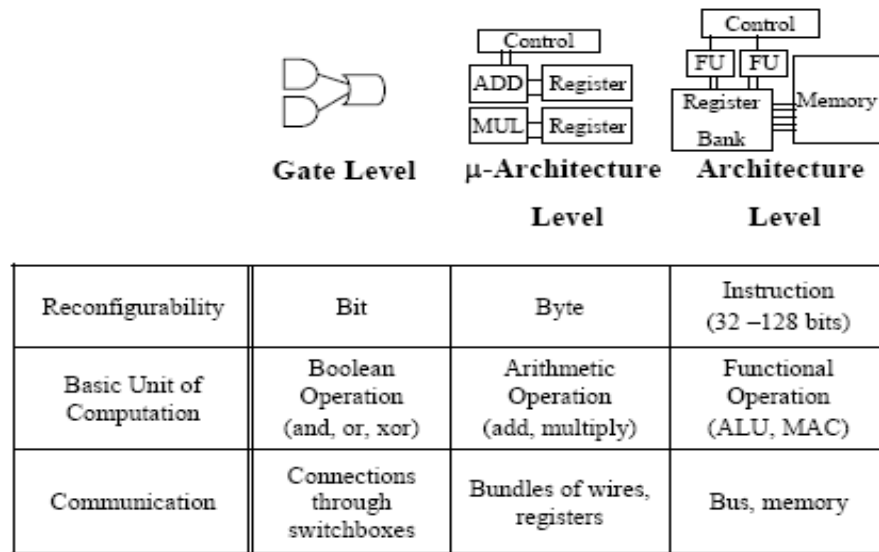


Figure 2. Comparisons of 3 levels of computational hierarchy¹¹(From Betz and Rose)

a. ASIC to PLD

As shown in Figure 3 below, the family of programmable devices encircles many forms of logic devices. The initial offerings created to achieve programmability were the forerunners to the sophisticated devices that followed. To achieve the promise of reconfigurable hardware, programmers began in the early stages of development, operating with the programmable logic device (PLD). This device was able to provide “post-fabrication configuration”.¹² The PLD could combine many

¹¹ Kia Barzargan, *Synthesis Techniques and Optimizations for Reconfigurable Systems* Editor, 2006.

¹² Vaughn Betz and Jonathan Rose., *FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density*.

characteristics of the nonprogrammable ASIC into a more efficient device. At that stage of early development, a key parameter was flexibility and with the PLD, this could be achieved because the connection between the programmers and physical connections required only simple programming. However, the “PLD proved to be time consuming in operating and generated several layers of delay overhead”.¹³

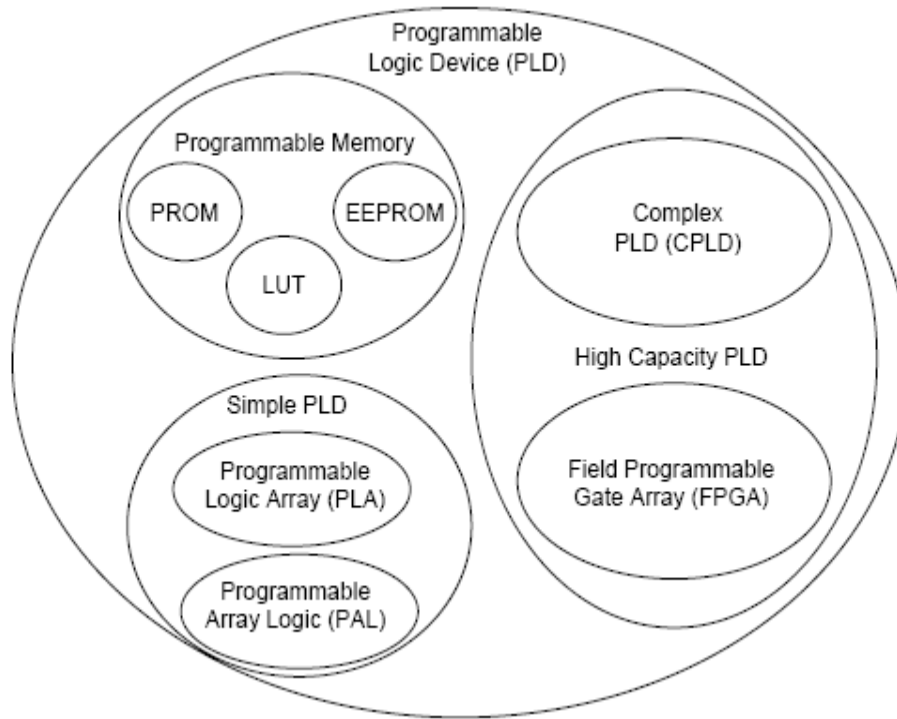


Figure 3. Overview of programmable devices¹⁴(From Barzargan)

b. PLD to PGA

As technology advanced, developers sought ways to design devices that were more efficient. The ASIC made way for the PGA, which created the market place for quick easy design items, which greatly shortened the design process. There were ways to ensure the PGA development process would not be jeopardized by delays and typical

¹³ Vaughn Betz and Jonathan Rose., *FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density*.

¹⁴ Barzargan, *Synthesis Techniques and Optimizations for Reconfigurable Systems*.

increased power consumption of the newer devices. These two factors alone are very important considerations in the development of reconfigurable circuitry.

c. PGA to FPGA

As stated, the need for programmability led to design changes in the early PGA devices. A key component in the programmable equation is the flexibility the device achieves. As the PGA advanced what emerged was a device, the FPGA, “that provided an order of magnitude of programmable bits compared to an average microprocessor”.¹⁵ A relevant aspect of the “potential benefits of the FPGA is the correlation between the number of programming bits and flexibility of a logic device as well as system performance, which provides greater power dissipation and energy usage compared with an ASIC.”¹⁶

2. Architecture Design and Classification

The FPGAs design provides the AEGIS system many benefits. Figure 4 below shows a typical FPGA in use today. Let us start with the two modes of operation performed by the device; download and configure. “The download mode updates the devices memory and the configure mode runs the device as specified by its configuration.”¹⁷ With these modes came a decreased configuration time when compared to older devices.

¹⁵ Vaughn Betz and Jonathan, Rose., *FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density*

¹⁶ Ibid.

¹⁷ Ibid.



Figure 4. An Altera Stratix II GX FPGA ¹⁸(From Wei and Chan)

Figure 5 below shows the basic type of routing architecture showing a pass gate. This gate was the necessary connection between routing channels. Many of the first generation FPGAs were designed with this basic architecture, but as they have advanced, they now employ the more sophisticated “island style routing architecture” shown below in Figure 6. “The two styles of architecture are distinguishable by the number of wires that make up a single logic block, the older models had only a single length wire, and the newer island style models have a combination of length 1 wires and up to eight length wires spanning eight logic blocks.” This logic blocks configuration could provide the device a considerable increase in power and speed which is necessary for operation in the AEGIS system.

¹⁸ Hsiung Wei and Roy Chan, Performance analysis of IEEE 802.11a signals under different operational environments, M.S. in Electrical Engineering, Naval Postgraduate School, 2004, (Monterey, California: 91.

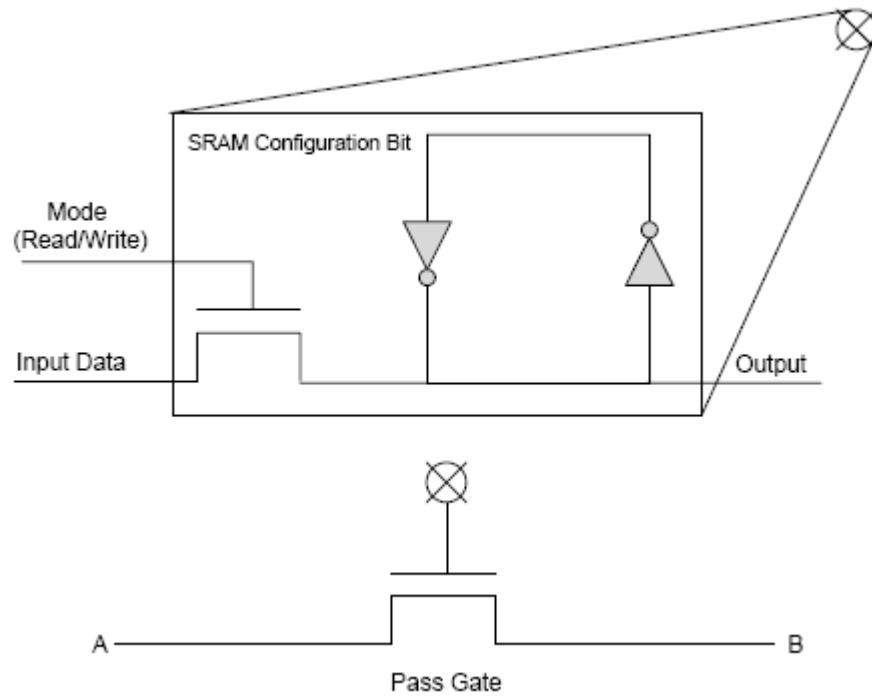


Figure 5. Generic routing architecture¹⁹(From Barzargan)

¹⁹ Barzargan, *Synthesis Techniques and Optimizations for Reconfigurable Systems*.

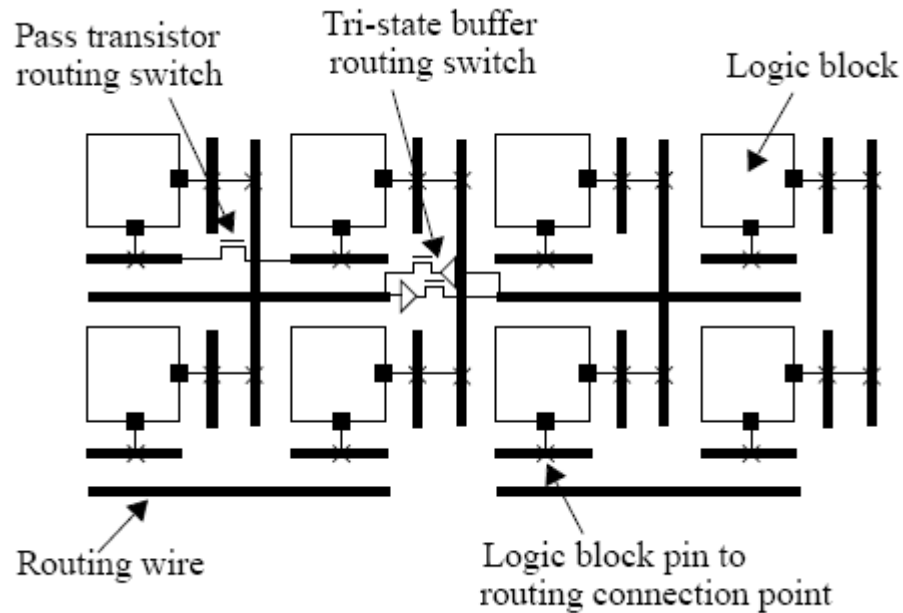


Figure 6. Island style routing architecture²⁰(From Betz and Rose)

a. Reprogrammable Look up Table

A significant difference between the FPGA, from previous gate arrays and generic microprocessors is its use of the Reprogrammable Look up Table (LUT). The LUT provides three of the most beneficial parameters necessary within the AEGIS weapon system, the ability to be reprogrammed, upgraded, and interoperability. With the use of LUTs, the system, consisting of FPGAs as the core computing components are capable of operating together in several types of missions. For example, engineers at Sky Computers, lead by Steve Paavola, see a distinct advantage during synthetic aperture radar (SAR) missions. Mr. Paavola states, “On an unmanned aerial vehicle surveillance mission, operators may have to reconfigure the sensors on the fly based on changing mission parameters, weather conditions, etc.” Figure 7 shows the LUT and its makeup up consisting of many switches to perform varying modes of operation.

²⁰ Vaughn Betz and Jonathan Rose. "FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density."

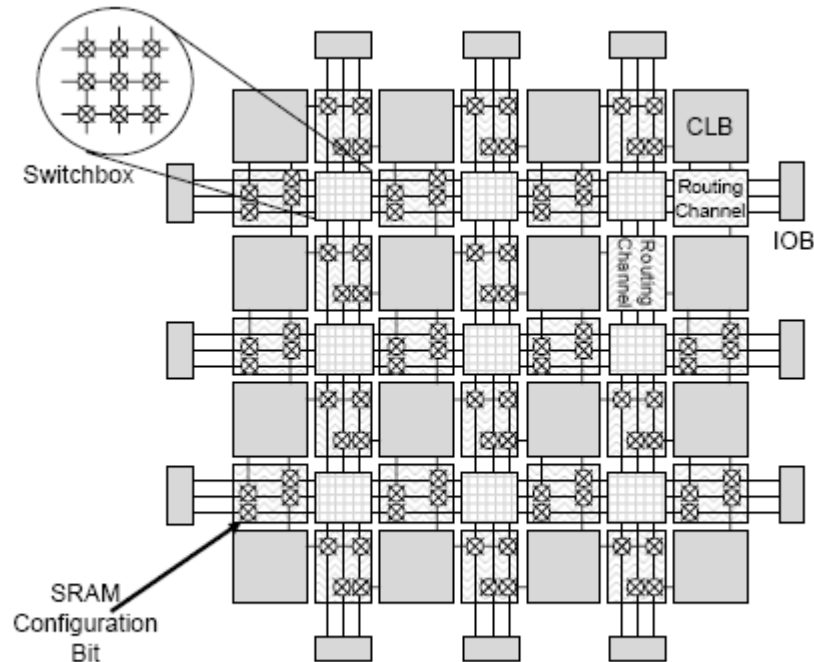


Figure 7. LUT switchboxes for varying modes of operation ²¹(From Betz and Rose)

b. Reconfigurable Granularity

The benefits that FPGAs are capable of achieving are due to another key parameter; granularity. Many devices such as the FPGA are considered “fine grain architecture”. “Granularity is the ability to reconfigure a devices abstraction level.”²² The abstraction level is directly related to the length of its configuration time. Granularity is inversely related to configuration time; therefore, with the FPGA being a high granularity device, it has a short configuration time. To restate how important this key parameter is, the ability to reconfigure the FPGA during a critical mission is shorter than previous hardware components.

²¹ Vaughn Betz and Jonathan Rose., *FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density*.

²² Barzargan, *Synthesis Techniques and Optimizations for Reconfigurable Systems*.

3. Performance

For the system operators and technicians of AEGIS, how the FPGA performs its mission may be a significant factor in utilizing the devices. The FPGA is substantially more efficient and capable of performing many functions when compared to its predecessors. Because the devices are programmable, they can be reconfigured efficiently and quickly.

Generally, programmers have a preferred FPGA for programmable gates, the SRAM. If the SRAM FPGA is used, its ability for reconfiguration is a trade off for its volatility, a system restart results in the need for reprogramming the device. Volatility is not a significant threat because the devices are designed and configured efficiently.

Current commercial FPGAs are capable of being used in several forms that could be beneficial to the way in which the IWS would utilize them. These FPGAs are capable of high processing speeds critical to shipboard operators relying on the system update to achieve interoperability.

4. Reconfigurability

What makes the FPGA such a useful device in the AEGIS system is its ability to be reconfigured. The term reconfigurability is generally defined as “any information processing system in which blocks of hardware can be reorganized or repurposed to adapt to changing data flows or algorithms”.²³ Unlike a microprocessor, which cannot be reconfigured the FPGA can change its function to adapt to its environment.

5. Power Consumption

The devices are remarkable, but do have some immediate design specifications that must be addressed. The FPGA device must be capable of consuming less power than its predecessors consume. To accomplish this task the devices must remove glitches, or “unnecessary transitions or hazards”.²⁴ Programmers have determined a way to remove

²³ Barzargan, *Synthesis Techniques and Optimizations for Reconfigurable Systems*.

²⁴ Ibid.

glitching, which involves the addition of more devices capable of being programmed. “FPGAs are capable of aligning the arrival times of early arriving signals to the inputs of the lookup tables (LUTs) and to filter out glitches generated by earlier circuitry.”²⁵ Whenever glitches are removed, so is power. However, glitch reduction comes at a price of area and speed overhead. “As the glitches are minimized the amount of power dissipated by FPGAs, referred to as dynamic power, seems to occur during toggling of the circuit nodes as detailed by a recent study.” The study examined power dissipation and found that “dynamic power accounted for 62% of total power in FPGA circuitry.”²⁶ As glitches are reduced, delay in the circuitry is reduced as well. “With an average elimination of 91% of glitching, overall FPGA power is reduced by 18.2% while added circuitry increases overall area by 5.3% and critical path delay by only 0.2%.”²⁷ In Table 1, the first column shows a typical circuit with glitching. The second column shows realizable power saving by eliminating glitching without overhead. “The potential power savings range between 4% and 73%, with an average savings of 22.6%; this is great motivation to reduce glitching in FPGA circuitry.”²⁸

Power (mW) (glitching)	Power (mW) (no glitching)	% Difference
24.3%	18.8%	22.6%

Table 1. FPGA Power Dissipation With and Without Glitching²⁹(From Barzargan)

²⁵ Barzargan, *Synthesis Techniques and Optimizations for Reconfigurable Systems*.

²⁶ Ibid.

²⁷ Ibid.

²⁸ Ibid.

²⁹ Ibid.

C. POTENTIAL BENEFITS OF FPGA COMPONENTS

1. Implementation of Hardware/Software Partitioning

From previous topics on how the FPGA is capable of performing in several modes of operation and what it can provide in the AEGIS weapon system, a fundamental aspect in the design of the system as shown in Figure 1 was the complete partitioning of hardware and software components. Partitioning in this sense is concerned with how the system components are separated to perform their assigned tasks. For the FPGA this would allow it to be reconfigured to carry out its mission and optimize resource utilization. Tasks assigned to a specific application are important in the design and use of FPGA technology in AEGIS, which is what the device provides.

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III. AEGIS BASELINES AND LEGACY COMPONENTS

A. AEGIS LEGACY COMPUTER SYSTEMS

1. AN/UYK 7 and AN/UYK 43 Systems

The standard legacy computers used in the original AEGIS baselines were the first generation UYK-7 computers. These consisted of integrated circuit boards and 32-bit processors. Figure eight below shows the circuit board and the pins used to mount the board to a chassis.

As increased processing power and cache memory were needed, the UYK 43 on later AEGIS baseline ships replaced the UYK 7. The processing power of the UYK 43 was more than the UYK 7 but it still included only a 32-bit processor. The newer computers were highly capable for the non-tactical data systems (NTDS) of the AEGIS platforms.

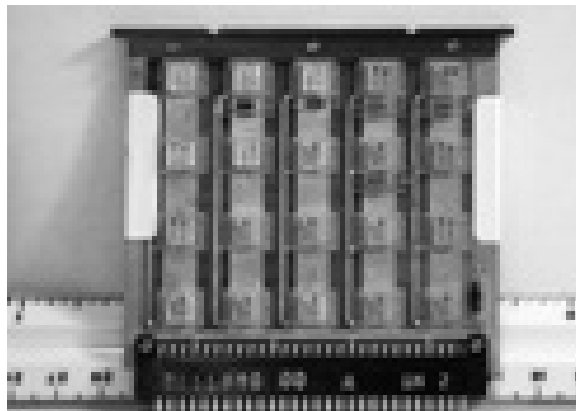


Figure 8. UYK 7 printed circuit board³⁰(From McHale)

³⁰ John McHale, AEGIS BMD weapon system with prototype signal processor tracks ballistic missiles, 2006).

a. Upgradeability of the Standard Computer

The original standard UYK-7 and UYK-43 computer systems were closed systems, which relied on limited, expensive, and extensive upgrades. The costs associated with upgrading the proprietary AEGIS components were a contributing factor leading the Navy towards the OA acquisition approach.

The computer systems, UYK-7 and UYK-43, of AEGIS handle all the necessary computations. As technology advanced, the computers required more power and expensive upgrades. The upgrades were extensive because they involved the “spaghetti code” of serial or point-to-point computing. To effectively upgrade the code required the entire system to be tested regardless of what function was upgraded. Any inadvertent change to one function could not be allowed because of an upgrade to another. This expensive proposition to upgrading AEGIS forced the service to look towards OA and open system architecture. Naval planners understood faster computers were not the answer, and needed an overall movement away from closed to open system procurement.

The standard computer systems were capable of performing the necessary missions of AEGIS but as the need for greater computing power increased, the systems were incapable of keeping pace. One problem of upgrading had to do with the amount of time and resources the process took. The old systems were incapable of performing varying missions and to configure them for diverse roles required long lead times to ensure the necessary upgrades would be available in time. These systems have a fraction of the processing power of newer open systems, which allow for varying modes of operation on a single board.

Each upgrade to the legacy systems applied to keep pace with advancing technology created several baselines of AEGIS ships in the fleet, leading to seven baselines. A baseline is simply a specific configuration of the system dependent on the types of software, which are used in the system, whether the system uses the UYK 7 or upgraded UYK 43 and UYK 44, and the variant of the SPY 1 radar installed onboard. The heart of the AEGIS weapon system is the SPY 1 radar. The phased array radar is

capable of tracking upwards of 100 targets simultaneously for missions that include anti air, anti submarine, and anti ship. “AEGIS is so advanced that its computers must perform between 10 million to 20 million actions every second.”³¹

The AEGIS upgrades are increasingly important as the mission of the AEGIS ships is changing to be included in the ballistic missile defense (BMD) system. It has become a global effort to confront the threat of ballistic missiles and the Navy leadership has been aware that AEGIS would play an integral part.

B. BALLISTIC MISSILE DEFENSE

1. System Components and Functions

The Ballistic Missile Defense (BMD) mission aspects of the AEGIS system are increasingly important; therefore, the ability of AEGIS to perform at the highest level must be addressed. The service has initiated a plan towards BMD capable ships, as illustrated in Table 2. The ships are differentiated by either having a long-range search and track (LRS &T) capability or the ship is fully modified to become Engage-capable. To redesign current AEGIS ships with the BMD capability engineers would update the computer programs, which give SPY the ability to detect and track ballistic missiles and arm the ship with the latest version of the standard missile.

³¹ Sandra I. Erwin, Navy to Upgrade Aegis Ships with Open Software Standards, May 2003.

	Cumulative total by end of calendar year					
	2004	2005	2006	2007	2008	2009
<i>LRS&T ships</i>						
CG-47s	1	0	0	0	0	0
DDG-51s	5	9	10	8	1	0
Subtotal	6	9	10	8	1	0
<i>Engage-capable ships</i>						
CG-47s	0	2 ^a	3	3	3	3
DDG-51s	0	0	3	6	14	15
Subtotal	0	2 ^a	6	9	17	18
<i>Total LRS&T Engage-capable ships</i>						
	6	11	16	17	18	18

Table 2. AEGIS BMD Installation Schedule³²(From O'Rourke)

2. FPGA Usage in the BMD System

The FPGA, with its fast computing, ease of upgrades, and reconfigurability would allow for increased capabilities in the ballistic missile defense system. Older proprietary computers, with limited power, are incapable of performing varying functions simultaneously. In April 2007, tests conducted onboard USS Lake Erie (CG 70), under the supervision of Lockheed Martin representatives, proved the effectiveness of the open system processors, which were capable of detecting and tracking ballistic missile threats with a prototype of a Ballistic Missile Defense Signal Processor (BSP). The tests were successful because the newer chips in the BSP can perform the work of thousands of standard Navy computers. The prototype used the precursor to the FPGA that was scheduled to be incorporated into later tests.

³² Ronald O'Rourke, Sea Based Ballistic Missile Defense- Background and Issues for Congress, (2007).

IV. LIFE CYCLE COSTS AND BENEFITS OF FPGA'S TO AEGIS UPGRADE

A. RETURN ON INVESTMENT COMPARATIVE ANALYSIS

1. ROI Definition

ROI is defined several ways for varying organizations. “The ROI in assets is a measure of performance that is determined by the percentage relationship of earnings to assets.”³³ The ROI in any organization, such as those in the civilian sector, “could define the term in this basic equation”.³⁴

$$\text{ROI} = \frac{(\text{Gain from Investment} - \text{Cost of Investment})}{\text{Cost of Investment}}$$

This formula simply states that to calculate ROI, “the benefit (return) of an investment is divided by the cost of the investment; the result is expressed as a percentage or a ratio”.³⁵ The attainment of a high positive ROI for an organization indicates a very efficient use of assets.

This formula fits well in the public and civilian sectors where the organization produces revenue, part of the numerator of the ROI equation. For the Navy, a non-revenue producer, ROI cannot simply be measured with the same approach. So how does the Navy determine whether the FPGA is beneficial to its aging AEGIS fleet?

2. Cost Benefits

The costs benefits of upgrading the AEGIS system have potential savings of billions of dollars in the end. The cost benefit of utilizing programmable devices such as

³³ Clarence B. Nickerson, Accounting Handbook for Nonaccountants. 3rd Ed. New York: Van Nostrand Reinhold Co., 1986. p. 73.

³⁴ Clarence B. Nickerson, Accounting Handbook for Nonaccountants. 3rd Ed. New York: Van Nostrand Reinhold Co., 1986. p. 632.

³⁵ Answers.com, ROI, Copyright © 2007 Answers Corporation.

the FPGA as compared to legacy computing systems, UYK 7 or UYK 43, is illustrated in Figure 9. The figure compares the cost and volume of devices. The FPGA offers significant benefits in reducing costs for the future AEGIS system.

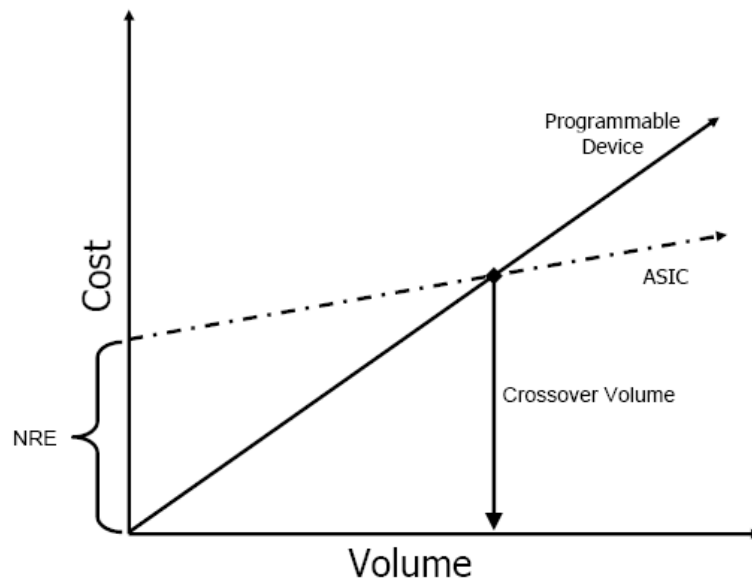


Figure 9. Cost vs. Volume of ASIC and programmable devices³⁶(From Answers.com)

The proposed budgets for AEGIS modernization which focus on BMD includes first, upgrading the SPY 1 radar and its signal processors to allow for tracking and engaging highflying ballistic missiles and secondly, the deployment of an upgraded standard missile 3 (SM-3 Block 1A). The upgraded signal processors would allow the best chance to intercept a launched ballistic missile during the initial phase of launch when the ballistic missile is more vulnerable to detection. FPGA hardware could be a main improvement to the signal processors and their ability to carry out such a mission.

Figure 10 below shows variations in costs for the AEGIS prime contractor for BMD in 2004. The figure shows the “variance”, which is any deviation from the proposed budget. A positive variance is considered good and a negative variance is considered bad. The proposed budget, for calendar year 2004 was \$6 billion dollars. As the prime contractor for the AEGIS system upgrade, Lockheed Martin was over \$3

³⁶ Answers.com, ROI, Copyright © 2007 Answers Corporation.

million dollars under budget for the year. As advances in the technology continue and Lockheed outsources contracts to other vendors costs should remain low. The costs included research development and testing of the AEGIS system as it shifts from the standard computer technology towards an open architecture open system consisting of FPGA devices.

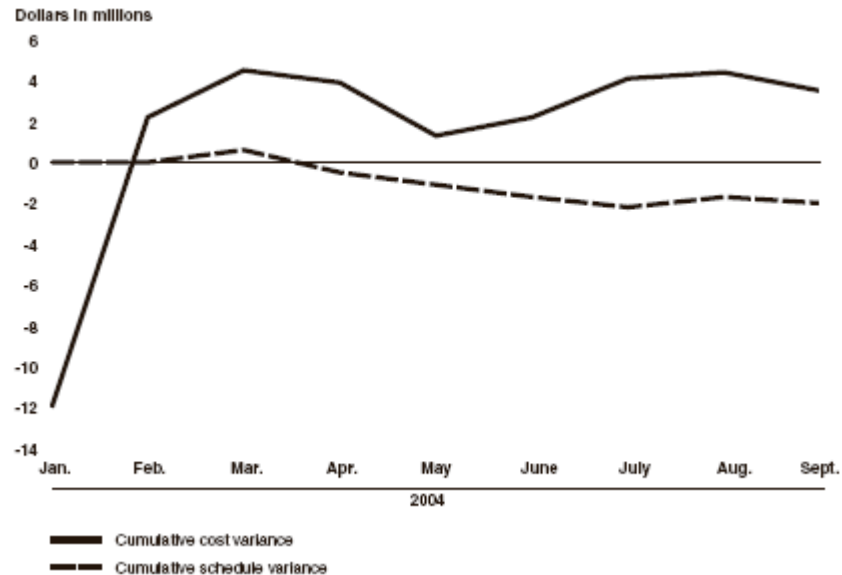


Figure 10. Prime contractor costs and schedule variances (From GAO)³⁷

The benefits achieved from open architecture procurement of FPGA devices can be seen in reduced hardware maintenance time. This reduction involves communicating programming upgrades to the FPGA or troubleshooting and sending error corrections. A reduction in overall ship operating costs, between \$1 and \$2 million dollars, associated with upgrading closed computing systems, which require periodic maintenance from civilian contractors traveling out to a ship at sea. The possibility of reduced crew sizes and even a reduction in the number of AEGIS ships because the FPGA devices can be monitored from shore sites capable of providing distance support to ships. These ships would be better suited to perform various types of missions because of FPGA devices.

³⁷ GAO, Missile Defense: Actions Are Needed to Enhance Testing and Accountability, [GAO-04-409](#) (Washington, D.C.: Apr. 23, 2004).

The increased capabilities of BMD engaged capable ships would ensure a modernized fleet capable of carrying out varying missions. These are all key elements in hardware upgrades similar to previous and ongoing software upgrades using open architecture.

3. Adler and Ahart Thesis Research

In June 2007, the team of J. Adler and J. Ahart researched the use of OA in sustaining engineering in AEGIS ships. The thesis looked at one aspect of OA, upgrading the software, not hardware, and how it could benefit the Navy in its search for a less expensive alternative to upgrading the system. Their findings were highly encouraging because they concluded OA is indeed the best practice, as compared to current configurations.

a. Positive ROI

As stated, one goal of a ROI measurement is to find a positive percentage when comparing expenses and revenue. Adler and Ahart looked at both return on knowledge (ROK), the efficiency in which processes utilize assets and control expenses for OA software upgrades, and ROI for future upgrades. Their work on OA software upgrades provides a comparative analysis into the benefits of OA hardware upgrades with the FPGA. Table 3 below summarizes their findings in which “the savings the Navy could expect were nearly 30 million dollars with a positive ROI near 72287% for the entire fleet of AEGIS ships.”

Process	Revenue	Total Costs	ROI
New Release Fielded (Push to Ship via Distance Support)	\$ 23,887,034.88	\$ 7,150.50	333681%
Remote Diagnostics Detect/Fix Anomaly	\$ 198,891,955.86	\$ 50,319.38	395159%
Remote Diagnostics Submit Software Bug Report for Anomaly	\$ 47,734,069.36	\$ 1,430.10	3337713%
Anomaly Verified	\$ 4,773,406.94	\$ 17,021.50	27943%
Anomaly Appended to Working List of Known Issues	\$ 1,414,342.80	\$ 1,307.00	108113%
Workaround Developed	\$ 2,545,817.03	\$ 17,021.50	14856%
New Software Version Developed	\$ 12,729,085.16	\$ 236,750.00	5277%
Known Anomalies are Resolved	\$ 4,972,298.89	\$ 100,638.75	4841%
New Software Version Fielded to Units (Pushed to Ship via Distance Support)	\$ 25,458,170.32	\$ 13,723.50	185408%
Totals	\$ 322,386,180.83	\$ 445,362.23	72287%

Table 3. ROI for all AEGIS ships³⁸ (After Adler and Ahart)

³⁸ Jameson R. Adler and Jennifer Ahart, AEGIS Platforms: Using KVA Analysis To Assess Open Architecture in Sustaining Engineering, Master's Thesis, Naval Postgraduate School, 2007.

b. Recommendations and Findings³⁹

Their recommendations are summarized below.

- The use of OA components in AEGIS allow for easier remote monitoring and upgrades to the system's software components
- Software upgrades through the OA process are delivered to the operational units faster than those that relied on the closed process
- The ROI achieved through the process is so significant that any future upgrades to the process could be substantial

Adler and Ahart's findings are beneficial for this thesis work on OA at the hardware level because it illustrates what an upgrade on AEGIS hardware could mean. "Naval estimates have the costs to upgrade a single AEGIS cruiser are about \$221 million and for an AEGIS destroyer the cost is \$ 78 million with a total costs for the entire fleet of AEGIS ships at \$9.7 billion."⁴⁰ With these numbers, the findings show that an upgrade to the standard computers today costs between \$1 to \$2 million dollars each, not including the time it actually takes to perform the upgrade. This is one issue when shifting from closed systems, which are not cost effective. Newer FPGAs, which are reconfigurable and therefore easier to upgrade with less down time are more cost effective. Another key aspect concerning the cost effectiveness of the FPGA is its ability to be reprogrammed on the fly with programming commands capable of being sent to a ship at sea from a shore location.

FPGAs provide significant advantages to OA upgrades of the AEGIS system. Naval leadership continues to show growing interests in extending the service life of its AEGIS fleet and the findings are indicative of the benefits the service life extensions would be compared to the costs of upgrading the closed systems. This would

³⁹ Jameson R. Adler and Jennifer Ahart, AEGIS Platforms: Using KVA Analysis To Assess Open Architecture in Sustaining Engineering, Master's Thesis, Naval Postgraduate School, 2007.

⁴⁰ Ronald O'Rourke, *Navy Aegis Cruiser and Destroyer Modernization: Background and Issues for Congress*. (The Library of Congress: , 2007) (Accessed 8/14/2007).

be similar in nature and should be considered further by Navy planners. Work is already underway to incorporate the FPGA due to its tremendous benefits in terms of power, performance, and changing functionality.

As stated, the FPGA provides several advantages over standard Naval computing systems. These advantages include the costs required to update and reconfigure the system dependent on the mission it is required to perform and their ease of design and quick production. The use of FPGA technology in AEGIS will provide a long-term costs reduction for the Navy and its ship development. Critics could argue that the idea of a positive ROI are not applicable to the Navy and the risks of incorporating such technology could be costlier by not looking at alternative means. The facts support the notion that as an organization, the Navy must adhere to strict budget guidelines and therefore keep its operating costs low and maximize its budget.

B. SHIP LIFE CYCLE EXTENSIONS

“The Navy has proposed FY2008 budget requests \$474.5 million for the modernization of its AEGIS cruisers and destroyers.”⁴¹ The overall plan calls for the use of OA to improve the combat capabilities and reduce operating costs, which include maintenance and upkeep. For the AEGIS fleet the goal is “to keep the ships in service for a period of 35 years to 40 years”.⁴²

The plan for the modernization of the cruiser and destroyer fleet is without its critics. The need to continue the funding for the next generation warship is an idea that continues to spread throughout the Congress, as some ask why the service should continue to spend on upgrading the ageing fleet at the expense of the future combat ships.

⁴¹ Ronald O’Rourke Navy AEGIS Cruiser and Destroyer Modernization: Background and Issues for Congress, the Library of Congress, 2007.

⁴² Ronald O’Rourke Navy AEGIS Cruiser and Destroyer Modernization: Background and Issues for Congress, the Library of Congress, 2007.

1. Cruiser (CG)

The AEGIS cruiser has long been the workhorse of the fleet. The Navy has planned “to upgrade 22 cruisers and keep them in service to age 35”.⁴³ The need for improved combat capabilities and ships that are less expensive to operate and maintain is a key decision the Navy has made as it has decommissioned earlier baseline cruisers to costly to upgrade.

2. Destroyer (DDG)

The DDG-51 modernization plan calls for 62 ships to be upgraded. A smaller vessel compared to the cruisers, the DDG eventually will replace the cruiser as the AEGIS workhorse in the fleet. Because it deploys with less crew and has lower costs associated with operation, the Navy has much interest in how long to keep the ships in service.

3. LCS and DD(X)

The next generation warship would benefit greatly from the OA concept in its operations and maintenance environment. “OA could be a utilized in creating a common combat system across this and other surface ships, such as aircraft carriers, amphibious ships, and LCSs.”⁴⁴

⁴³ Ronald O’Rourke Navy AEGIS Cruiser and Destroyer Modernization: Background and Issues for Congress, the Library of Congress, 2007.

⁴⁴ Ronald O’Rourke Navy AEGIS Cruiser and Destroyer Modernization: Background and Issues for Congress, the Library of Congress, 2007.

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V. CONCLUSION AND RECOMMENDATIONS

A. CONCLUSION AND RECOMMENDATIONS

The Navy has long realized the benefits that OA provides, and it continues to improve the process of using COTS in its surface ships. With the ageing of the AEGIS cruiser and destroyer fleets, the need for a new approach to achieve the greatest combat effectiveness in its next generation ships can become a reality.

The proposed budget to provide the AEGIS system with BMD capabilities has shown that the prime contractor, Lockheed Martin, was capable of reducing costs associated with hardware upgrades. The cost reduction of \$3 million dollars in 2004 was encouraging because as the technology advances and outsourcing of contracts increases, competition in open architecture procurement will result in fewer costs to the service. As shown Adler and Ahart's thesis, the service could see savings approaching \$30 million dollars directly attributable with software upgrades and could see further savings in the future.

The FPGA is a device that will greatly improve the AEGIS weapon system. As the Navy continues with the OA approach to acquisition and the benefits of hardware upgrades by using the reconfigurable and reprogrammable FPGA, the service will undoubtedly see serious cost savings and a positive ROI.

By contracting out the design and implementation of the FPGA device in the BMD system, the Navy will see an increased performance capability in its designated ships. The Navy can move forward into the next generation ships with the knowledge that the FPGA is one device that can provide its AEGIS ships the power and performance demanded of it.

B. RESEARCH LIMITATIONS

This research is limited by the inability to see the FPGA device in use with the AEGIS system. The Navy's transformation to FPGA devices will begin shortly as the

contracted company, Lockheed Martin, continues to outsource the procurement of faster computing devices. A representative for Lockheed Martin stated in April 2007, “It would take thousands of UYK 43s to perform the capabilities of the BSP”,⁴⁵ the prototype BMD signal processor that performed successful tests which will eventually include the FPGA.

⁴⁵ John McHale, *AEGLS BMD Weapon System with Prototype Signal Processor Tracks Ballistic Missiles.*, 2006), www.mae.pennet.com (accessed 8/12/2007).

VI. FUTURE RESEARCH

A. FUTURE RESEARCH

Future research in on this topic should focus on the actual use of FPGA devices in the AEGIS system. Current testing by Lockheed Martin and other vendors are quickly moving towards the use of FPGAs in conducting BMD exercises. Researchers and designers see a promising future for the AEGIS systems and this includes the FPGA.

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